昆貿電子股份有限公司

QUEEN MAO ELECTRONIC CO., LTD.

Multi-Layer Ceramic Chip Capacitors Specifications (MLCC Series)

Approved by: Frank Kao

File Number:	QM-C-01 (E)	Quality Control Stamp
Version:	1	
Pages:	17	
Effective Date:	Mar. 01, 2004	
Written by:	Paul Chang	
Edited by:	Frank Kao	

NOTE	

Topic	Page

Ordering Code

CC	0805	Y	104	Z	3	S	B	T
①	②	③	④	⑤	⑥	⑦	⑧	⑨

① Style

CC: MLCC

② Chip Size: L´W

0402=0.04×0.02”
0603=0.06×0.03”
0805=0.08×0.05”
1206=0.12×0.06”
1210=0.12×0.10”
1812=0.18×0.12”

④ Capacitance

In pF, the first two digits are significant digits and the last digit gives the no. of zeros.

8=×0.01
9=×0.1
0=×1
1=×10
2=×100
3=×1000
4=×10000

Example:
278:0.27pF
471:470pF
103:0.01uF

⑤ Tolerance

A:	±0.05pf	H:	±3%
B:	±0.10pf	J:	±5%
C:	±0.25pf	K:	±10%
D:	±0.50pf	M:	±20%

③ Dielectric Material

N: NPO
X: X7R/X5R
Z: Z5U
Y: Y5V
U: Y5U

⑥ Rated Voltage

A	=	10Vdc
B	=	6.3Vdc
C	=	250Vdc
1	=	16Vdc
2	=	25Vdc
3	=	50Vdc
4	=	100Vdc
5	=	200Vdc
6	=	500Vdc
7	=	1KVdc
8	=	3KVdc

⑦ Termination Style

O: Cu/Ni/Sn
S: Ag/Ni/Sn

⑧ Chip Thickness

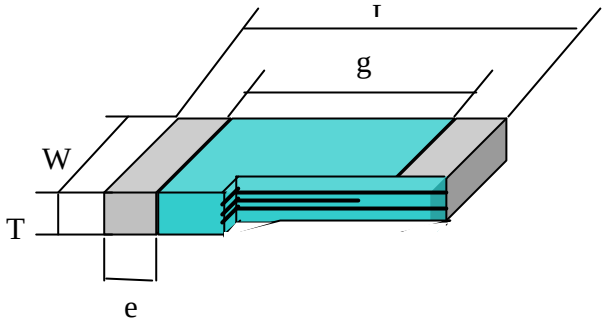
S: 0.50mm±0.05mm(0402)
S: 0.80mm±0.10mm(0603)
A: 0.6±0.1mm
B: 0.8±0.1mm
C: 1.0±0.1mm
D: 1.15±0.1mm
E: 1.25±0.1mm
F: 1.60±0.15mm
G: 1.90±0.15mm
H: 2.10±0.15mm
T: > 2.25mm

⑨ Packing Standard

B: Bulk
T: Paper Tape
R: Plastic Tape

Remarks:
When place order, please clear indicate ① ~ ⑥ (⑦ ~ ⑨ can be leaved out).

Chip Capacitor Structure



Size	**L** Length inch (mm)	**W** Width inch (mm)	**e(min)** Termination inch (mm)	**g(min)** Insulation inch (mm)
0402	0.04±0.002 (1.0±0.05)	0.02±0.002 (0.5±0.05)	0.0059~0.0118 (0.15~0.3)	0.0157 (0.4)
0603	0.063±004 (1.6±0.1)	0.032±0.003 (0.8±0.1)	0.0079~0.0196 (0.2~0.5)	0.0196 (0.5)
0805	0.079±0.004 (2.0±0.1)	0.049±0.004 (1.27±0.1)	0.0079~0.0276 (0.2~0.7)	0.0591 (1.5)
1206	0.126±0.006 (3.2±0.15)	0.063±0.006 (1.6±0.15)	0.0118 min (0.3 min)	0.0394 (1.0)
1210	0.126±0.006 (3.2±0.15)	0.098±0.006 (2.5±0.15)	0.0118 min (0.3 min)	0.0787 (2.0)
1812	0.177±0.010 (4.5±0.25)	0.126±0.006 (3.2±0.15)	0.0118 min (0.3 min)	0.0787 (2.0)

	Code	Thickness(mm)
0402	S	0.50mm±0.05mm
0603	S	0.80mm±0.10mm
0805/1206	A	0.6±0.1mm
0805/1206	B	0.8±0.1mm
0805/1206/1210	C	1.0±0.1mm
0805/1206/1210	D	1.15±0.1mm
0805/1206/1210/1812	E	1.25±0.1mm
1206/1210/1812	F	1.60±0.15mm
1210/1812	G	1.90±0.15mm
1210/1812	H	2.10±0.15mm
1210/1812	T	＞2.25mm

ELECTRICAL CHARACTERISTICS

Dielectric Material

Material	Tolerance	Characteristics	Application
NPO (COG)	1) A,B,C,D,F,G 2) J,K prefered	Class I Low K dielectric : extremely stable in capacitance regardless of time and temperature change, With low dielectric loss and small tolerance on nominal capacitance.	Precision timing circuits, high frequency noise filtering impedance matching, ESD Limiting.
X7R X5R	1) J 2) K,M prefered	Class II middle K dielectric: allowing higher capacitance than Class I dielectric in less stable frequency, voltage, and temperature condition.	Noise filtering, frequency discrimination, by-pass and decoupling in radio receivers, audio tone, and computer serve system.
Z5U Y5V Y5U	1) K 2) M,Z prefered	Class II High K dielectric: allowing high capacitance density as a replacement of tantalum, aluminum electrolytic capacitor.	Low frequency noise by-pass and high speed power decoupling application.

Capacitor Classification

Classification of ceramic based capacitor

By refer to EIA standard, ceramic capacitors are break down into three categories:

CLASS I: COG(NPO), also called “temperature compensation” type, It is temperature stable or compensating device, it shows very little or no changes in capacitance as temperature change, suitable for timing, impedance matching, ESD/EMI limiting.

CLASS II: X7R,Z5U,Y5V,also called “high K”type, those materiala present greater capacitance change than class I type, a variety of dielectric materials are available thus the amount of capacitance change is to be defined from vendor to vendor.

CLASS III: is semiconductor type which exhibit capacitance change similar to class II’s , however, this type is very rare in consumer application.

Aging Phenomenon

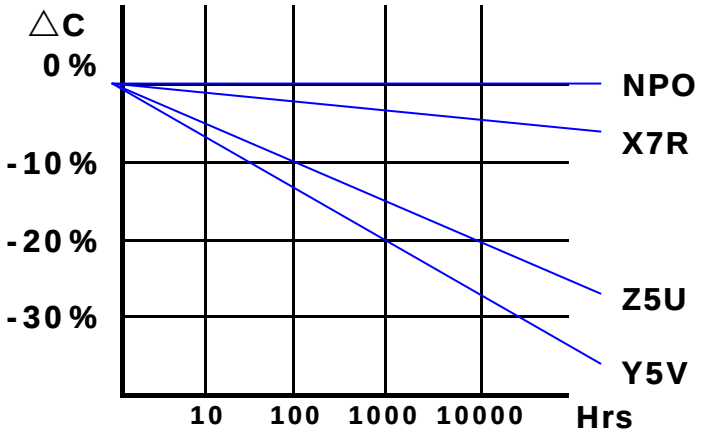
What is aging of class II ceramic (change of capacitance over time)
Aging is the Shelf-Loss in capacitance that occurs over time and is a normal process of class II ceramic capacitors, because of the re-ordering of crystalline structure
When a class II ceramic body is cool from its Curie Point @150℃ and without voltage applied, then the aging starts under a given ratio designated by vendor.
The average aging ratio (per $10^{\times}$ time decade)

NPO 0

X7R/75R≦2.5%

Z5U≦5%

Y5V/Y5U≦7%



Recovery of aging

1) heat up to device @150℃ or above, the higher temperature the less time required.
2) Voltage slows very much the aging behaviors of class II ceramic capacitor.

Handle guidelines of aging part

1) The aging parts will not lead to any reliability issue, but capacitance out from its lower limit which might be observed prior to production.
2) After de-aging process, the parts would back to its initial designated level of capacitance characteristic and another aging cycle begins when parts putting back to the storage shelf.
3) Typically, a process of IR reflow or wave soldering can easily recure the aging part since it all working at much higher temperature than 150℃, even few seconds dwelling time is far enough for staying at such 210℃~260℃ range.
4) Remeasurement of de-aging parts, must to wait at least 24 hours @ room temperature. While the part has cool down, then the capacitance is stable and shall be well within ts normal limit.

TESTS AND REQUIREMENTS

Item	Condition of test	Performance of requirement
Operating Temperature		NPO:-55℃~125℃ X7R:-55℃~125℃ X5R:-55℃~85℃ Z5U:+10℃~85℃ Y5V/Y5U:-30℃~85℃
Capacitance	NPO:≦1000pF,F=1MHz,V=1.0±0.2Vrms ＞1000pF,F=1KHz,V=1.0±0.2Vrms Z5U: F=1KHz,V=0.5V±0.2Vrms X7R/X5R/Y5V/Y5U F=1KHz,V=1.0V±0.2Vrms	Within specified tolerance
Dissipation Factor	Same condition as capacitance	NPO: Cap≧30pF, Q≧1000 Cap＜30pF, Q≧400＋20C X7R/: Rate Voltage 25V:≦2.5% X5R Rate Voltage 16V:≦3.5% Rate Voltage 10V:≦5% Z5U: All≦3.5% Y5V/: Rate Voltage 50V:≦5% Y5U Rate Voltage 25V:≦7% Rate Voltage 16V:≦9% Rate Voltage 10V:≦12.5%
Withstanding Voltage	DC voltage 250% of the rated voltage is applied between the terminations for 1 to 5 seconds, the charge and discharge current is less than 50mA.	No mechanical breakdown
Insulation resistance	Applying the rated voltage for 1 minute.	10000MΩ or 500ΩF minimum
Aging	Sit the capacitor at room temperature for 1000±12 hours, then measure. Perform a heat treatment at 140~150℃ for one hour and then let sit for 48±4 hours at room temperature .perform the initial measurement.	Capacitance change-Aging rate(ΔC%/decade hour) X7R/X5R-----Within ±2.5% Z5U-----Within ±5% Y5V/Y5U-----Within ±7%

<table>
<tr><th>Item</th><th>Condition of test</th><th>Performance of requirement</th></tr>
<tr><td>TCC</td><td>(1) temperature compensating type
using the capacitance measured in step 3 as a reference. Then cycling the temperature sequentially from step 1 to 5.
(2) high dielectric constant type
using the capacitance measured in step 3 as a reference. Then cycling the temperature sequentially from step 1 to 5.
<table><tr><td>Step</td><td>Temperature (℃)</td></tr><tr><td>1</td><td>25±2</td></tr><tr><td>2</td><td>Min. operating temp.±3</td></tr><tr><td>3</td><td>25±2</td></tr><tr><td>4</td><td>Max. operating temp.±3</td></tr><tr><td>5</td><td>25±2</td></tr></table></td><td><table><tr><td>Char.</td><td>Temp. range.</td><td>Reference. Temp.</td><td>Cap. Change</td></tr><tr><td>NPO</td><td>-55~+25</td><td rowspan="7">25</td><td>0.58%~ -0.24%</td></tr><tr><td>NPO</td><td>+25~+125</td><td>±30PPM /℃</td></tr><tr><td>X7R</td><td>-55~+125</td><td>±15%</td></tr><tr><td>X5R</td><td>-55~85</td><td>±15%</td></tr><tr><td>Z5U</td><td>+10~+85</td><td>+22%~ -56%</td></tr><tr><td>Y5V</td><td>-30~+85</td><td>+22%~ -82%</td></tr><tr><td>Y5U</td><td>-30~+85</td><td></td><td>+22%~ -56%</td></tr></table></td></tr>
<tr><td>Endurance</td><td>Apply 200% of the rated voltage for 1000±12 hours at the maximum operating temperature ±3℃.
Recovery: 24±2 hours

Special preconditioning for class 2 only
Apply 200% of the rated voltage for one hour at the maximum operating temperature ±3℃.
Recovery: 24±2 hours</td><td><table><tr><td>Char.</td><td>Cap.change</td></tr><tr><td>NPO</td><td>Within ±3% or±0.3pF max.</td></tr><tr><td>X7R/ X5R</td><td>Within ±12.5%</td></tr><tr><td>Z5U</td><td>Within ±30%</td></tr><tr><td>Y5V/ Y5U</td><td>Within ±30%(cap.<1.0μF)</td></tr><tr><td>Y5V</td><td>Within +30% ~ -40%
(cap.≧1.0μF)</td></tr></table>Q for class 1 only<table><tr><td>Cap.</td><td>Requirement</td></tr><tr><td>≧30pF</td><td>Q≧350</td></tr><tr><td>10pF~30pF</td><td>Q≧275+5/2C</td></tr><tr><td>≦10pF</td><td>Q≧200+10C</td></tr></table>DF for class 2 only(max)<table><tr><td>Char.</td><td>25V min</td><td>16V</td><td>10V</td><td>6.3V</td></tr><tr><td>X7R/ X5R</td><td>0.05</td><td>0.07</td><td>0.07</td><td>0.075</td></tr><tr><td>Z5U</td><td>0.04</td><td>-</td><td>-</td><td>-</td></tr><tr><td>Y5V/ Y5U</td><td>0.075</td><td>0.1 (c<1.0μF)
0.125 (c≧1.0μF)</td><td>0.15</td><td>0.15</td></tr></table>IR
More than 1000 MΩ or 50ΩF min.
Dielectric strength
No failure</td></tr>
</table>

<table>
<tr><th>Item</th><th>Condition of test</th><th>Performance of requirement</th></tr>
<tr><td>Damp heat</td><td>Apply the rated voltage for 1000±12 hours at 40±2℃ and 90 to 95% RH.
Recovery: Class 1 : 1~2 h
Class 2: 24±2 h

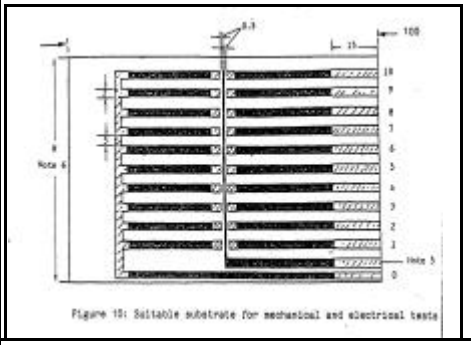
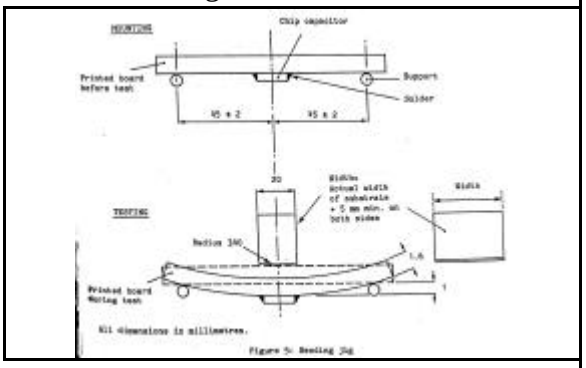
Special preconditioning for class 2 only
Apply the rated voltage for one hour at 40±2℃ and 90 to 95% RH.
Recovery: 24±2 hours</td><td>
<table>
<tr><th>Char.</th><th>Cap.change</th></tr>
<tr><td>NPO</td><td>Within ±7.5% or±0.75pF max.</td></tr>
<tr><td>X7R/ X5R</td><td>Within ±12.5%</td></tr>
<tr><td>Z5U</td><td>Within ±30%</td></tr>
<tr><td>Y5V/ Y5U</td><td>Within ±30%(cap.<1.0μF)</td></tr>
<tr><td>Y5V</td><td>Within +30% ~ -40% (cap.≧1.0μF)</td></tr>
</table>
Q for class 1 only
<table>
<tr><th>Cap.</th><th>Requirement</th></tr>
<tr><td>≧30pF</td><td>Q≧200</td></tr>
<tr><td>≦30pF</td><td>Q≧100+10/3C</td></tr>
</table>
DF for class 2 only(max)
<table>
<tr><th>Char.</th><th>25V min</th><th>16V</th><th>10V</th><th>6.3V</th></tr>
<tr><td>X7R/ X5R</td><td>0.05</td><td>0.07</td><td>0.07</td><td>0.075</td></tr>
<tr><td>Z5U</td><td>0.05</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Y5V/ Y5U</td><td>0.075</td><td>0.1 (c<1.0μF)
0.125 (c≧1.0μF)</td><td>0.15</td><td>0.15</td></tr>
</table>
IR: More than 500 MΩ or 25ΩF min.
Dielectric strength: No failure</td></tr>
<tr><td>Temp. cycle</td><td>Perform the five cycles according to the four heat treatments listed in the following table.

Recovery: 24±2 h

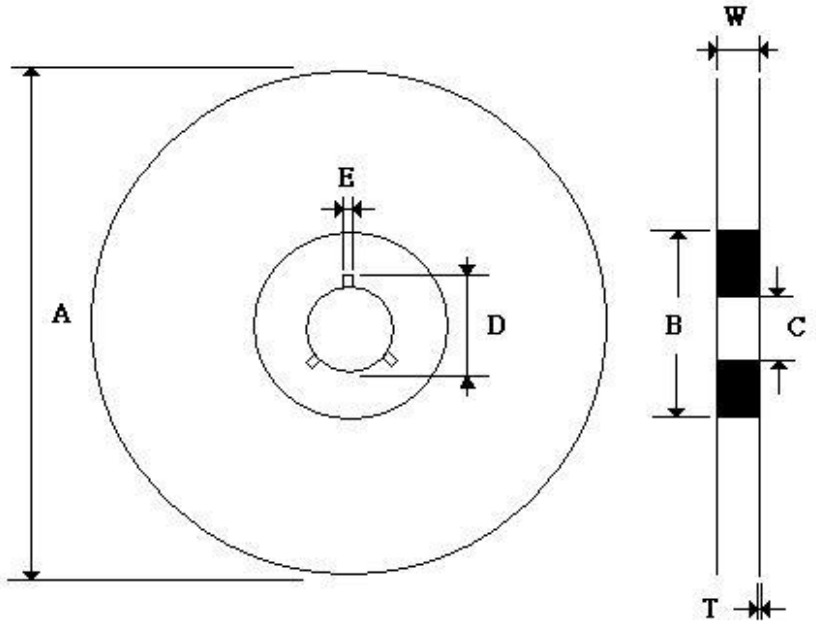
Special preconditioning for class 2 only
Apply a heat treatment at 150~140℃ for one hour .
Recovery: 24±2 hours</td><td>
<table>
<tr><th>Char.</th><th>Cap.change</th></tr>
<tr><td>NPO</td><td>Within ±2.5% or±0.25pF max.</td></tr>
<tr><td>X7R/ X5R</td><td>Within ±7.5%</td></tr>
<tr><td>Z5U</td><td>Within ±20%</td></tr>
<tr><td>Y5V/ Y5U</td><td>Within ±20%</td></tr>
</table>
Q for class 1 only
<table>
<tr><th>Cap.</th><th>Requirement</th></tr>
<tr><td>≧30pF</td><td>Q≧1000</td></tr>
<tr><td>≦30pF</td><td>Q≧400+20C</td></tr>
</table>
DF for class 2 only(max)
<table>
<tr><th>Char.</th><th>25V min</th><th>16V</th><th>10V</th><th>6.3V</th></tr>
<tr><td>X7R/ X5R</td><td>0.025</td><td>0.035</td><td>0.05</td><td>0.05</td></tr>
<tr><td>Z5U</td><td>0.035</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Y5V/ Y5U</td><td>0.05</td><td>0.07 (c<1.0μF)
0.09 (c≧1.0μF)</td><td>0.125</td><td>0.125</td></tr>
</table>
IR: More than 10000 MΩ or 500ΩF min.
Dielectric strength: No failure</td></tr>
</table>

<table>
<tr><th>Item</th><th>Condition of test</th><th>Performance of requirement</th></tr>
<tr><td>soldering heat</td><td>Preheat the capacitor at 120~150 ℃ for 1 minute. Immerse the capacitor in a eutectic solder solution at 270±5℃ for 10±0.5 seconds.

Recovery: 24±2 h

Special preconditioning for class 2 only
Apply a heat treatment at 150~140℃ for one hour .
Recovery: 24±2 hours</td><td>
<table>
<tr><td>Char.</td><td>Cap.change</td></tr>
<tr><td>NPO</td><td>Within ±2.5% or±0.25pF max.</td></tr>
<tr><td>X7R/ X5R</td><td>Within ±7.5%</td></tr>
<tr><td>Z5U</td><td>Within ±20%</td></tr>
<tr><td>Y5V/ Y5U</td><td>Within ±20%</td></tr>
</table>
Q for class 1 only
<table>
<tr><td>Cap.</td><td>Requirement</td></tr>
<tr><td>≧30pF</td><td>Q≧1000</td></tr>
<tr><td>≦30pF</td><td>Q≧400+20C</td></tr>
</table>
DF for class 2 only(max)
<table>
<tr><td>Char.</td><td>25V min</td><td>16V</td><td>10V</td><td>6.3V</td></tr>
<tr><td>X7R/ X5R</td><td>0.025</td><td>0.035</td><td>0.05</td><td>0.05</td></tr>
<tr><td>Z5U</td><td>0.035</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Y5V/ Y5U</td><td>0.07</td><td>0.09 (c<1.0μF)
0.125 (c≧1.0μF)</td><td>0.125</td><td>0.125</td></tr>
</table>
IR: More than 10000 MΩ or 500ΩF min.
Dielectric strength: No failure</td></tr>
<tr><td>Deflection</td><td>Capacitance(with printed board in bent position)
Visual examination
  </td><td>Capacitance decrease≦10%
No visible damage
  </td></tr>
<tr><td>Adhesion</td><td>Solder the capacitor as deflection. Then apply a 10N force in parallel with the test jig for 10±1 sec.</td><td>No removal of the terminations or other defects shall occur.</td></tr>
<tr><td>Solderability</td><td>Soldering temperature :230±5℃
Immersion time:2±1 sec</td><td>At least 95% of the terminal surface must be covered by new solder.</td></tr>
</table>

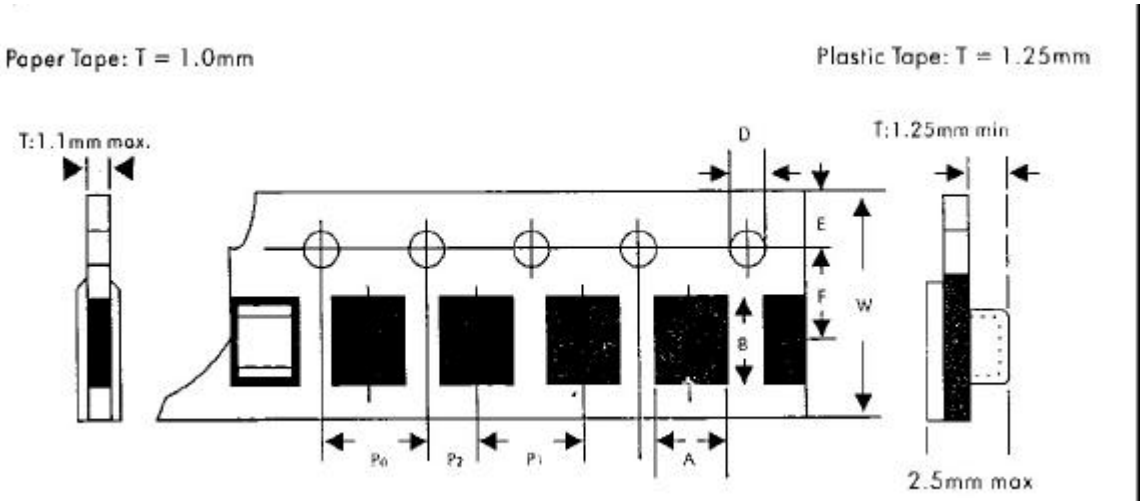
PACKAGING



Tape Size	A Max.	B Min.	C	D Min.	E Min.	W	T Max.
8mm	330 (12.992)	50 (1.969)	13.0±0.5 (0.512±0.02)	20.2 (0.795)	1.5 (0.059)	9±0.5 (0.354±0.02)	1 (0.04)
12mm						13±0.5 (0.512±0.02)	

STANDARD

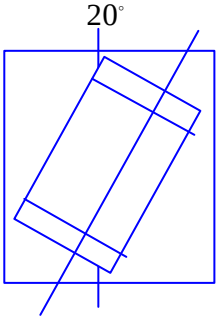
Size	7 Reel		13 Reel		Tape Width
	Paper	Plastic	Paper	Plastic	
0402	10,000		50,000		8mm
0603	4,000		15,000		
0805	4,000	3,000	10,000	10,000	
1206	4,000	3,000	10,000	10,000	
1210		3,000			12mm
1808		1,500 1,000			
1812		1,500 1,000			



	0402	0603	0805	1206	1210	1808	1812
A	0.6±0.05 (.024±002)	1.1±0.2 (.043±008)	1.5±0.2 (.059±008)	1.9±0.2 (.075±008)	2.8±0.2 (.110±008)	2.3±0.2 (.91±008)	3.5±0.2 (.138±008)
B	1.2±0.05 (.047±002)	1.9±0.2 (.075±008)	2.3±0.2 (.091±008)	3.5±0.2 (.138±008)	3.5±0.2 (.138±008)	4.9±0.2 (.193±008)	4.9±0.2 (.193±008)
D	1.5±0.1 (.059±004)	1.5±0.1 (.059±004)	1.5±0.1 (.059±004)	1.5±0.1 (.059±004)	1.5±0.1 (.059±004)	1.5±0.1 (.059±004)	1.5±0.1 (.059±004)
E	1.75±0.1 (.069±004)	1.75±0.1 (.069±004)	1.75±0.1 (.069±004)	1.75±0.1 (.069±004)	1.75±0.1 (.069±004)	1.75±0.1 (.069±004)	1.75±0.1 (.069±004)
F	3.5±0.1 (.138±004)	3.5±0.1 (.138±004)	3.5±0.1 (.138±004)	3.5±0.1 (.138±004)	3.5±0.1 (.138±004)	5.5±0.1 (.217±004)	5.5±0.1 (.217±004)
P0	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)
P1	2.0±0.05 (.079±002)	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)	4.0±0.1 (.157±004)	8.0±0.2 (.315±008)	8.0±0.2 (.315±008)
P2	2.0±0.05 (.079±002)	2.0±0.05 (.079±002)	2.0±0.05 (.079±002)	2.0±0.05 (.079±002)	2.0±0.05 (.079±002)	2.0±0.05 (.079±002)	2.0±0.05 (.079±002)
W	8.0±0.3 (.315±012)	8.0±0.3 (.315±012)	8.0±0.3 (.315±012)	8.0±0.3 (.315±012)	8.0±0.3 (.315±012)	12.0±0.2 (.472±008)	12.0±0.2 (.472±008)

COMPONENT ROTATION

Maximum Component Rotation



Component Center Line

Component Cavity Center Line

The Essence of a capacitor

THE SORTS OF DIELECTRIC MATERIAL FROM THEIR COMPONENTS.

1) Ceramic
2) Tantalum
3) Electrolytic Aluminum
4) Polymer, OS- Con etc.

Different type of capacitor has its characteristics and suitable for speciific applications,but NOT for unspecified.

HOW IS A MULTI LAYER CERAMIC CAPACITOR FORMED

A number of conductive electrodes lay-down(Pd / Ag / Ni / Cu) separated by an insulating dielectric sheet

CAPACITORS IN SERIES

1) 1/C total =1/ C1+1/C2+1/C3+ … 1/Cn
2) Respective current equally.

CAPACITORS IN PARALLEL

3) C total =C1+C2+C3+ … Cn
4) Respective voltage is equally.

STANDARD UNIT OF CAPACITANCE IS INDICATED AS "F OR FARAD"

μF = micro Farad = 10^{-6}

nF= nano Farad = 10^{-9}

pF = pico Farad = 10^{-12}

VOLTAGE AND AC

As a general rule, AC must not exceed 10% to the rated DC value.
If the AC voltage is too strong to the capacitor , the inner dielectric would heat-up and dissipation become an issue. Unusual AC spikes or surges will cause over heating and the dielectric would be ruptured or even on fire , This design rule should be strickly followed , particularly in the application above 1KHz switching frequency.

THE PARASTIC INDUCTANCE

Four contributed inductances

1)Component aspect ratio(chip length vs. width)

2)Circuit trace inductance

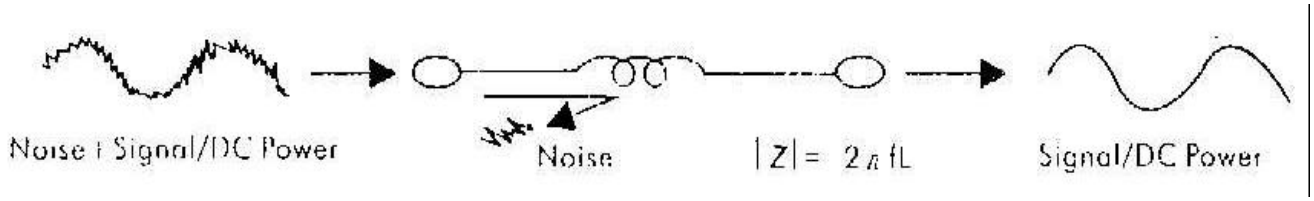
3)Via hole inductance

4)Packaging inductance

INDUCTIVE NOISE SUPPCESSION

When an inductor is inserted in series of a noise producing circuit, its impedance increases with frequency.

In this configuration, it is possible to attenuate and eliminate the noise components (high frequency components).

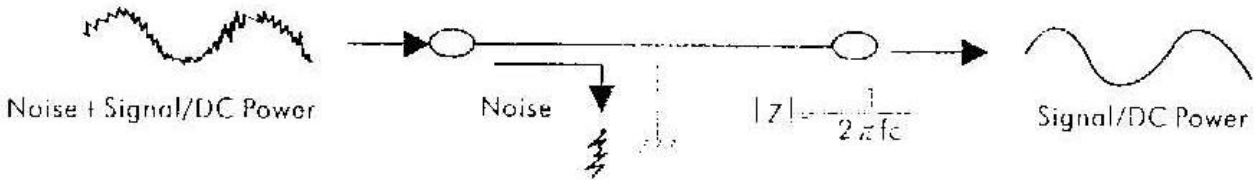


f : Frequency

L : Inductance value

CAPACITIVE NOISE SUPPRESSION

When a capacitor is connected (bypass capacitor) to ground from a noisy signal line or power line, the circuit impedance decreases as the frequency increases. Since noise is a high frequency phenomenon, it flows to ground. If a capacitor has been connected to ground, there by making it possible to eliminate noise.

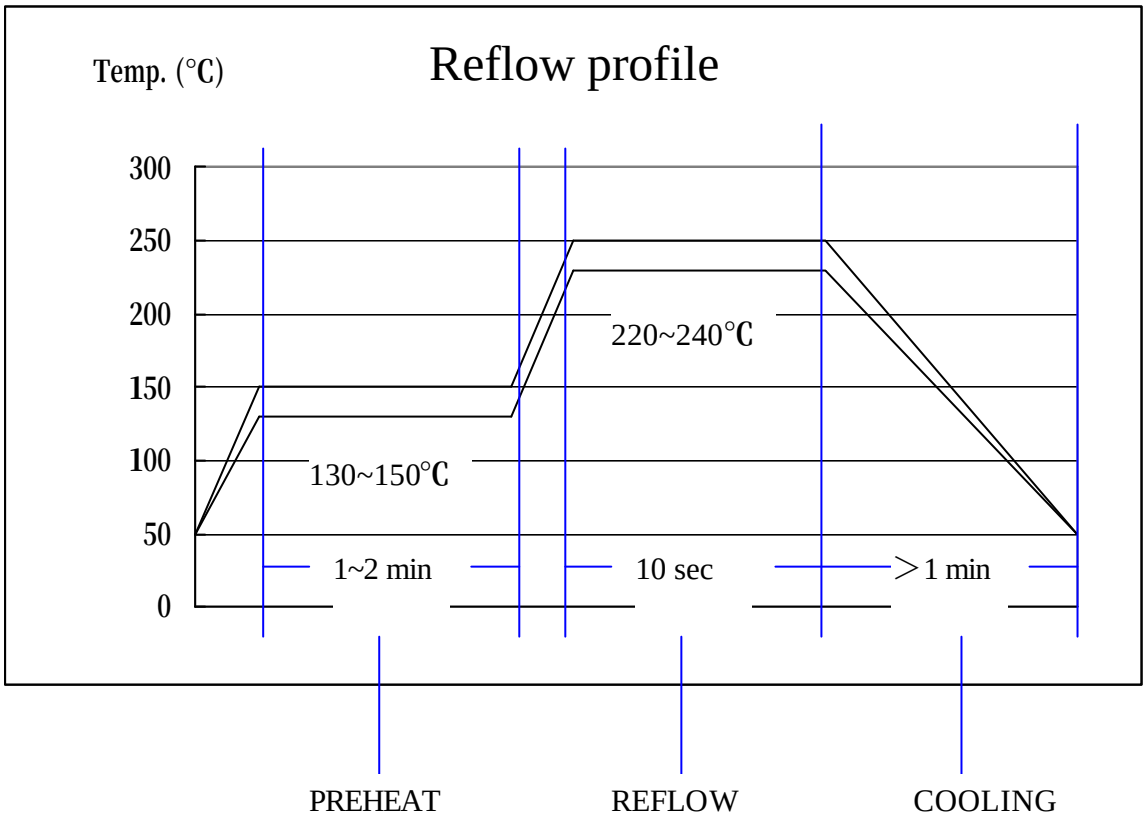


f : Frequency

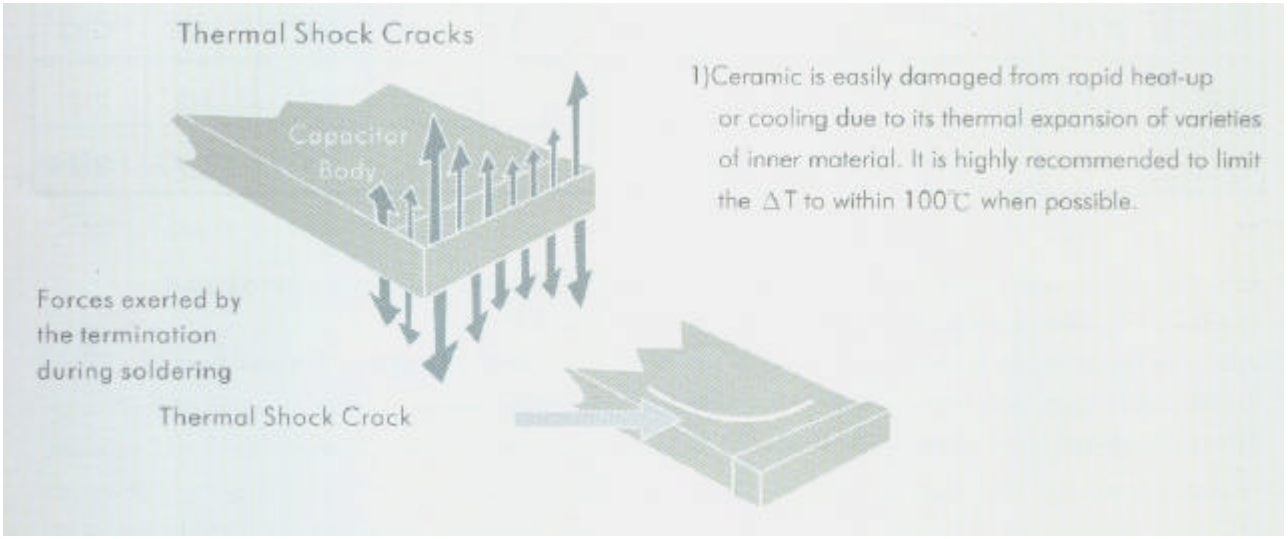
c : Capacitor value

Soldering Recommendation

Typical Profile Band for Sn63/Pb37 Alloy Solder Paste

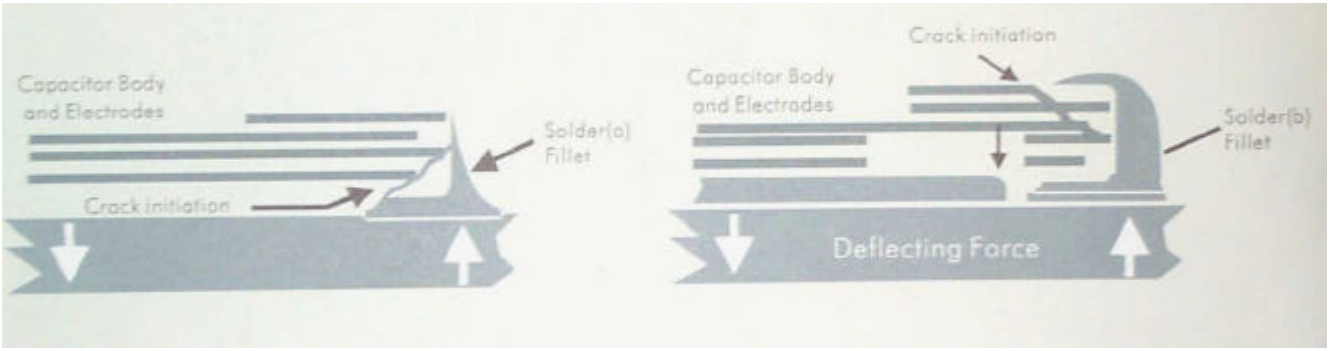


THERMAL SHOCK



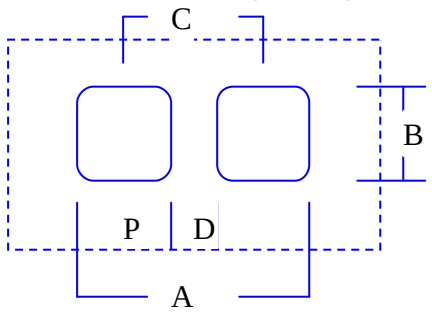
MECHANICAL DAMAGE

1)Board flexure cracks are common observed, especially manual breaking process is involved or large degree of PCB warpage exists at machine level handling.
2)The flexure crack can be eliminated by putting sensitive parts away from the high stress area. Position and orientation of the parts should be very important.



SOLDER PAD DESIGN GUIDES

(in case more details required, please reter to IPC 782 A)



	IR Reflow					Wave Solder				
Chip	A	D	B	P	C	A	D	B	P	C
*0402	2.14	0.28	0.74	(A-D)/2	A-P	N/A				
*0603	2.78	0.68	1.08	1.05	1.73	3.18	0.68	0.8	1.25	1.93
0805	3.30	0.70	1.6	1.3	2.0	3.7	0.7	1.1	1.5	2.2
1206	4.5	1.5	2.0	1.5	3.0	4.9	1.5	1.4	1.7	3.2

Note:*to minimize tombstoning for small chips 0402, 0603, four methodologies can be used
1)make all corners of the pads to round shape as above figure
2)Reduce the amount of solder paste using, a stencil opening which is less then the pad area
3)130~160 pre-heating temperature for more than 1 minute
4)controllthe pad size as small as possible

Terminology

CAPACITANCE:

C = eKA/t

CAPACITANCE TOLERANCE

is the amount of the actual capacitance allowed to deviate from the nominal value listed . For example , if you order a capacitor with a nominal of 1000pF and a tolerance of plus or minus 10%, you may get an actual value of 900 to 1100pF (at 25)

DISSPATION FACTOR (DF OR TAN d)

The amount of energy loss compared to that originally applied. DF is a measurement of how effective a capacitor is, DF = ESR/Xc

IRMS

Within a given temperature rise (10-20, typical), the maximum allowable AC to flow through a capacitor, the higher Irms the better heat dissipation of the capacitor.

Ims= √ESR/P

ESR

is accidentally built to non-ideal capacitor due to the material of inner electrodes and terminations . ESR = DF/2p fc

ESL

can also exists in non-ideal capacitor due to the aspect ratio (length vs. width of current path)

IZI

Is a combination of natural resistance and inductance properties . The total of these resistances is known as impedance. The amount of impedance to the current means determine it will pass or be blocked by the capacitor.

RATED VOLTAGE

All capacitors are rated for the amount of voltage which they can tolerate. By definition , voltage is the amount of pressure or force exerted on the current , to make the current move.

QUALITY FACTOR

Or "Q" , is the reciprocal of DF . if Q is high , the capacitor is considered as more effectively.

I . R.

Insulation Resistance comes from the dielectric and outer coating. If any, it is the only real resistance perceived by direct current , some DC leakage through the capacitor can occur . It depends on the capacitor's rating for IR . Ceramic Capacitors have relatively large IR ratings (1G or higher typically) than other dielectrics capacitor.

ALTERNATING CURRENT

AC is influenced by three resistances-ESR, inductance reactance XL and capacitive reactance XC. As a general rule, AC should not exceed 10% heat up and dissipation will become a problem, this is a particular true for above 1KHZ.

SELF RESONANT FREQUENCY

When a capacitor reaches a certain frequency where the capacitive reactance XC and inductance XL cancel each other out, when XC and XL cancel, the only impedance left is ESR and the current easily passes along in the circuit.

DIELECTRIC STRENGHT

When a rated voltage is given in percents form and defined the upper limits of voltage. The ceramic dielectric can tolerate without rupturing. It is a test measure only and is applied to assure reliability and integrity of the capacitor. It does not guarantee proper capacitor performance and should not be used to choose a capacitor. Except for rated voltage being used.

PHASE ANGLE Φ

POWER FACTOR =COSΦ OR SINd

D.F. = TANd